a stacked gate formed on the semiconductor body between the first and second semiconductor regions, with a gate insulating film inserted therebetween, the stacked gate having a first side surface, a second side surface opposed to the first side surface, and an upper surface;

an interlayer insulating film formed above the semiconductor body;

a contact material buried to be adjacent to the first side surface of the stacked gate in the interlayer insulating film, the contact material contacting the first semiconductor region;

a first insulating film formed on the second side surface and on the upper surface, but not on the first side surface of the stacked gate adjacent to the contact material; and

a second insulating film formed on the first side surface adjacent to the contact material, the second insulating film covering the entirety of the first insulating film.

5. (Amended) The device according to claim 1, wherein the first insulating film is an oxide-based insulating film having a film thickness of 100Å to 200Å, and the second insulating film is a nitride-based insulating film having a film thickness of 200Å to 400Å.

6. (Amended) A non-volatile semiconductor memory device comprising:

a semiconductor body of a first conductivity type;

first and second semiconductor regions of a second conductivity type, formed apart from each other on the semiconductor body;

a stacked gate formed on the semiconductor body between the first and second semiconductor regions, with a gate insulating film inserted therebetween, the stacked gate including a charge storage layer on the gate insulating film, a control gate on the charge storage layer, and a cap insulating film on the control gate, and the stacked gate having a first

side surface, a second side surface opposed to the first side surface, and an upper surface, the first and second surfaces each including side surfaces of the charge storage layer, the control gate, and the cap insulating film;

an interlayer insulating film formed above the semiconductor body;

a contact material buried to be adjacent to the first side surface of the stacked gate in the interlayer insulating film, the contact material contacting the first semiconductor region;

a first insulating film formed on the side surface of the control gate on the first side surface, and on all of the side surface of the charge storage layer on the first side surface; and

a second insulating film formed on the first side surface adjacent to the contact material, the second insulating film covering the entirety of the first insulating film.

9. (Amended) The device according to claim 6, wherein the first insulating film is an oxide-based insulating film having a film thickness of 100Å to 200Å, and the second insulating film is a nitride-based insulating film having a film thickness of 200Å to 400Å.

10. (Amended) A non-volatile semiconductor memory device comprising:

a semiconductor body of a first conductivity type;

first and second semiconductor regions of a second conductivity type, formed apart from each other on the semiconductor body;

a stacked gate formed on the semiconductor body between the first and second semiconductor regions, with a gate insulating film inserted therebetween, the stacked gate including a charge storage layer on the gate insulating film, a control gate on the charge storage layer, and a cap insulating film on the control gate, and the stacked gate having a first side surface, a second side surface opposed to the first side surface, and an upper surface, the

first and second surfaces each including side surfaces of the charge storage layer, the control gate, and the cap insulating film;

an interlayer insulating film formed above the semiconductor body;

a contact material buried to be adjacent to the first side surface of the stacked gate in the interlayer insulating film, the contact material contacting the first semiconductor region;

a first insulating film formed on the side surface of the control gate on the first side surface, on all of the side surface of the charge storage layer on the first side surface, on the side surface of the control gate on the second side surface, and on all of the side surface of the charge storage layer on the second side surface; and

a second insulating film formed on the first side surface adjacent to the contact material, the second insulating film covering the entirety of the first insulating film, the second insulating film being formed on the second side surface, and covering the entirety of the first insulating film and the upper surface.

13. (Amended) The device according to claim 10, wherein the first insulating film is an oxide-based insulating film having a film thickness of 100Å to 200Å, and the second insulating film is a nitride-based insulating film having a film thickness of 200Å to 400Å.

REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-13 are presently active. Claims 1, 5, 6, 9, 10, and 13 have been amended by the present amendment. Claims 14-18 have been withdrawn. The changes to the claims are supported by the originally filed specification and do not add new matter.